1) Simplify the following Boolean expression $[AB'(C+BD)+A'B']C$

A) $= [AB'C + AB'BD + A'B']C$

$= [A\bar{B}C + \bar{A}\bar{B}]C$

$= A\bar{B}C + \bar{A}\bar{B}C$

$= \bar{B}C(A+\bar{A})$

$= \bar{B}C$

2) $F(D,E,F) = D + E'F$

A)

D \ EF	$\bar{E}\bar{F}$	$\bar{E}F$	EF	$E\bar{F}$
$\bar{D}$		1		
D	1	1	1	1

$F(D,E,F) = \Sigma(1,4,5,6,7)$

3) What are clear & preset inputs initially configured as when JK Flip Flop is used as a down counter? Assume clear & preset are active low.

A) Clear is set to 0 & preset is set to 1.

4) What is decimal equivalent of octal number (37).

A) $(37)_8 = 3 \times 8^1 + 7 \times 8^0 = (31)_{10}$

5) What is Cin (input carry) pin of IC 7483 set to when it is used as 2's complement subtractor

A) Cin is set to 0.

6) Which statement below best describes a karnaugh map?

A) It is simply a rearranged truth table.

7) The simplified SOP form of the boolean expression $(P+Q'+R').(P+Q'+R).(P+Q+R')$ is

P	Q	R	Y
0	0	0	1
0	0	1	0
0	1	0	0
1	1	1	0
1	0	0	1
1	0	1	1
1	1	0	1
1	1	1	1

SOP; $\Sigma m(0,4,5,6,7)$

	$\bar{Q}\bar{R}$	$\bar{Q}R$	QR	$Q\bar{R}$
$\bar{P}$	1			
P	1	1	1	1

$\therefore$ SOP : $P+\bar{Q}\bar{R}$

8) Which of the following is not a weighted code?

A) excess 3. code.

9) A magnitude comparator is defined as a digital comparator which has

A) Three output terminals

10) Ring counter is analogous to

A) stepping switch

11) In Asynchronous UP counter, each flip flop is triggered

Ans) The normal output of the preceding flip flop.

12) A logic circuit that provides a high output for both inputs HIGH or both inputs LOW is.

A) Ex-Nor Gate.

13) In the toggle mode a JK flip flop has

A) J = 1 K = 1

14) Which of the following digital logic circuits can be used to add more than 1 bit simultaneously.

A) Ripple - carry adder.

15) When does a negetive level triggered flip flop in digital electronics changes its state?

A) when clock is low.

16) What must be used along with synchronous control inputs to trigger a change in flip flop?

A) Clock.

17) What will be the output from a D flip flop if clock is low & D = 0 ?

A) No change

18) Which are the universal gates in logic family?

A) NAND & NOR

19) What value is to be considered for "don't care cond".

A) either 1 or 0.

20) The minterm expansion of $f(A,B,C) = AB + BC' + AC$ is

	$B\bar{C}$	$\bar{B}C$	BC	$B\bar{C}$
$\bar{A}$				1
A	1		1	1

$\therefore m_2 + m_4 + m_6 + m_7$

21) The reduced SOP form of function $f(A,B,C,D) = \Sigma[m(1,3,7,11,15)]$ is.

	$\bar{C}\bar{D}$	$\bar{C}D$	CD	$C\bar{D}$
$\bar{A}\bar{B}$		1	1	
$\bar{A}B$			1	
AB			1	
$A\bar{B}$			1	

$\therefore \bar{A}\bar{B} + CD$

or

$CD + A'B'$

22) A 2 bit twisted ring counter cycles through

A) 4 states

23) In JK flip flop "no change cond" appears when

A) $J = 0, K = 0$

24) If A & B are the inputs of a half adder, the sum is given by.

A) A XOR B

25) If $J = K$ (J & K inputs are shorted) in a JK flip-flop what is the resulting device.

A) T flip flop.