Experiment / Assignment / Tutorial No. _____

Grade: AA / AB / BB / BC / CC / CD /DD

Signature of the Staff In-charge with date

Batch: A3	Roll No.: 16010121045	Experiment / assignment / tutorial No.: 8

Title: 4:1 Mux in VHDL

Objective: Design of 3 bit asynchronous counter using JK flip flop in VHDL

Expected Outcome of Experiment:

CO2: Use different minimization technique and solve combinational circuits, synchronous & asynchronous sequential circuits.

CO4: Implement digital networks using VHDL

Books/ Journals/ Websites referred:

- VLab Links: http://vlabs.iitb.ac.in/vlabs-dev/labs/dldesignlab/experimentlist.html
- R. P. Jain, "Modern Digital Electronics", Tata McGraw Hill
- M .Morris Mano, "Digital Logic & computer Design", PHI
- https://wiki.engr.illinois.edu/download/attachments/84770821/08-Multiplexers.pdf?version=2&modificationDate=1285128827000

Pre Lab/ Prior Concepts:

Multiplexer: Multiplexer is a special type of combinational circuit. It is a digital circuit which selects one of the n data inputs and routes it to the output. The selection of one of the n inputs is done by the select lines. To select n inputs we require m select lines, such that $2^m=n$. Depending on the digital code applied at the select inputs, one out of the n data sources is selected and transmitted to a single output . E is called as the strobe or enable input which is useful for cascading. It is generally on active low terminal that means it will perform the required operation when it is low. The multiplexer act like a digitally controlled single pole, multiple way switches. The output gets connected to only one input at a time. In most of the electronic system the digital data is available on more than one line. It is necessary to route the data over a single line, under such circumstances input at a time

Types of Multiplexer:

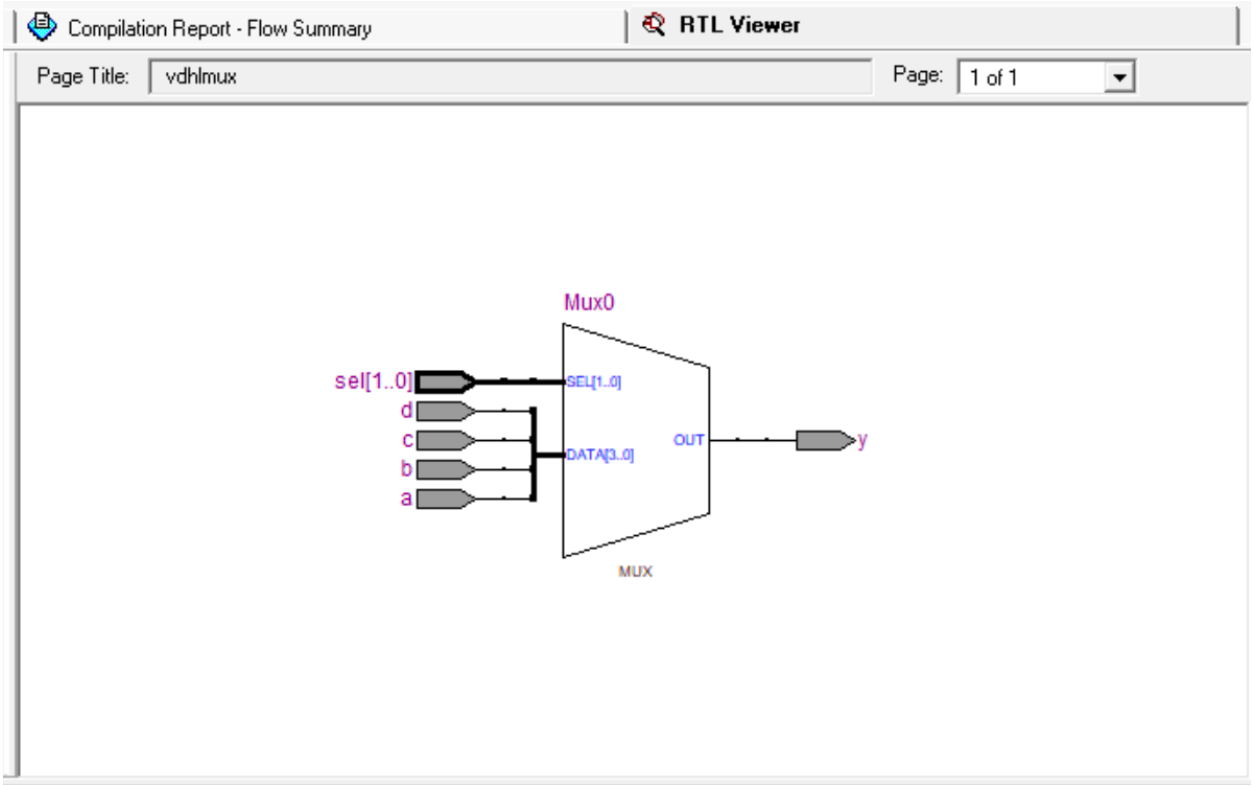
6. 2:1 Multiplexer

7. 4:1 Multiplexer
8. 8:1 Multiplexer
9. 16:1 Multiplexer
10. 32:1 Multiplexer

Implementation Details of 4:1 MUX

```
library IEEE;
use IEEE.STD_LOGIC_1164.all;
use IEEE.STD_LOGIC_arith.all;
use IEEE.STD_LOGIC_unsigned.all;
entity vhdlmux_test is -- entity of tb should be blank end vhdlmux_test;
--}} End of automatically maintained section architecture vdhlmux_test_arch of vhdlmux_test is
component vdhlmux is -- same as entity of your main code
port(
a,b,c,d:in std_logic;
sel :in std_logic_vector(1 downto 0);
y:out std_logic );
end component;

signal a,b,c,d,y : STD_LOGIC;

signal sel :std_logic_vector(1 downto 0);
begin
uut: vdhlmux port map (a,b,c,d,sel,y) ; --positional mapping process

begin -- write down the test cases

a<='0'; b<='0'; c<='1'; d<='1';
wait for 10ns;

sel <="00"; wait for 10ns;

sel <="01"; wait for 10ns; sel <="10"; wait for 10ns; sel <="11";

wait for 10ns;

 end process;

end ;
```

Screenshots



Conclusion: Hence**,** we successfully implemented mux in vhdl

Post Lab Descriptive Questions

1. Application Mux?

2. Multiplexers are used in various applications wherein multiple-data need to be transmitted by using a single line.
   Communication System
   A communication system has both a communication network and a transmission system. By using a multiplexer, the efficiency of the communication system can be increased by allowing the transmission of data, such as audio and video data from different channels through single lines or cables.
3. **Computer Memory**
4. Multiplexers are used in computer memory to maintain a huge amount of memory in the computers, and also to reduce the number of copper lines required to connect the memory

to other parts of the computer.

Telephone Network

5. In telephone networks, multiple audio signals are integrated on a single line of transmission with the help of a multiplexer.

Transmission from the Computer System of a Satellite

The multiplexer is used to transmit the data signals from the computer system of a spacecraft or a satellite to the ground system by using a GSM satellite.