Experiment / Assignment / Tutorial No. 6

Grade: AA / AB / BB / BC / CC / CD /DD

Signature of the Staff In-charge with date

Batch: A3	Roll No.: 16010121045	Experiment / assignment / tutorial No.: 6

Title: Shift Register

Objective: To implement the SISO, SIPO, PISO, PIPO shift register using D flips flop

Expected Outcome of Experiment:

CO2: Use different minimization technique and solve combinational circuits, synchronous & asynchronous sequential circuits.

Books/ Journals/ Websites referred:

- VLab Link: http://vlabs.iitkgp.ernet.in/dec/#
- R. P. Jain, "Modern Digital Electronics", Tata McGraw Hill
- M .Morris Mano, "Digital Logic & computer Design", PHI
- A.P.Godse, D.A.Godse, "Digital Logic Design"

Pre Lab/ Prior Concepts:

A register is capable of shifting its binary information in one or both directions is known as shift register. The logical configuration of shift register consist of a D-Flip flop cascaded with output of one flip flop connected to input of next flip flop. All flip flops receive common clock pulses which causes the shift in the output of the flip flop.The simplest possible shift register is one that uses only flip flop. The output of a given flip flop is connected to the input of next flip flop of the register. Each clock pulse shifts the content of register one bit position to right.

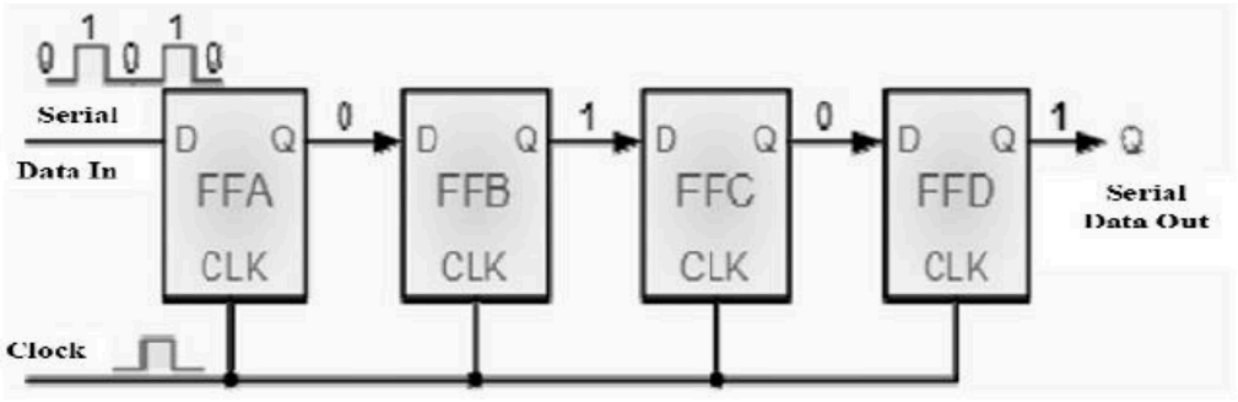
The basic types of shift registers are

- Serial In - Serial Out
- Serial In - Parallel Out
- Parallel In - Serial Out
- Parallel In - Parallel Out
- Bidirectional shift registers.

Implementation Details:

Logic Diagram

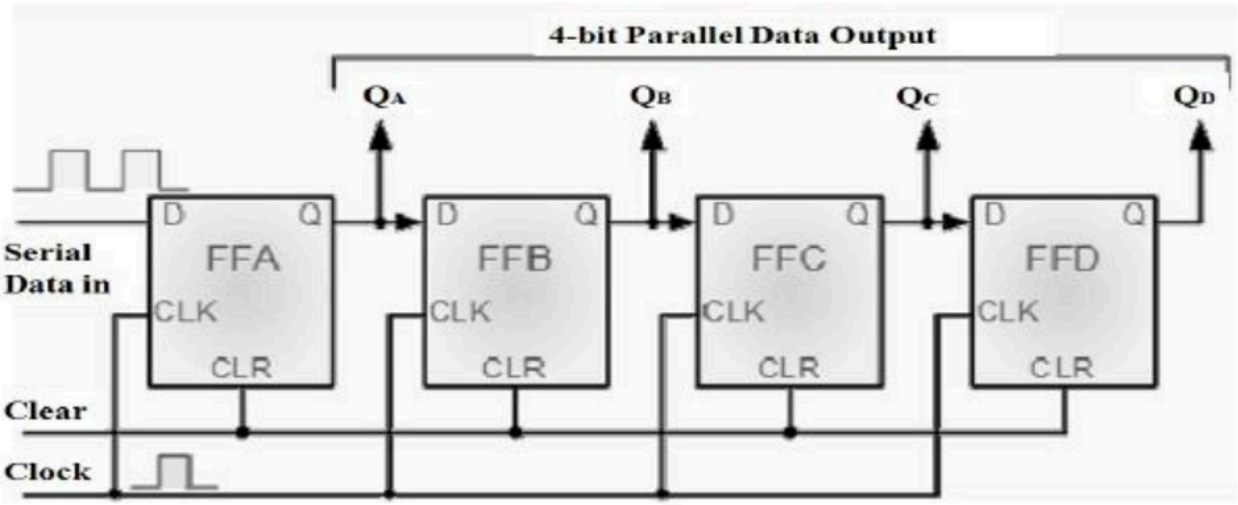
Serial in Serial Out



Truth table

CLK	D3	D2	D1	D0	Q3	Q2	Q1	Q0
0	0	0	0	0	0	0	0	0
1	0	0	0	1	0	0	0	1
2	0	0	1	1	0	0	1	1
3	0	1	1	0	0	1	1	0
4	1	1	0	1	1	1	0	1

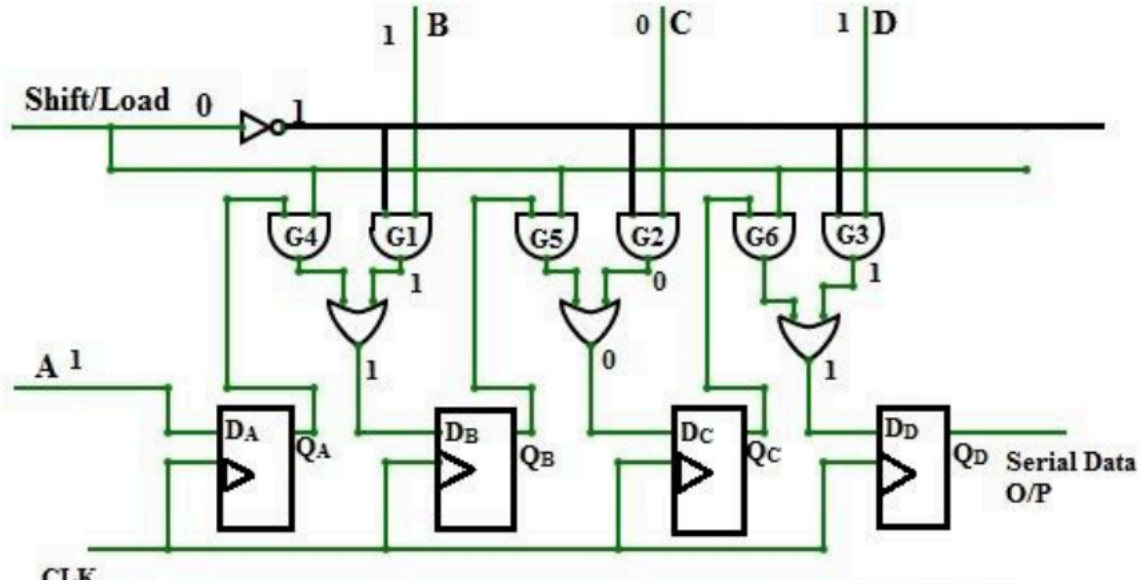
Serial In - Parallel Out



Truth table

CLK	D3	D2	D1	D0	Q3	Q2	Q1	Q0
0	0	0	0	0	0	0	0	0
1	1	0	0	0	1	0	0	0
2	0	1	0	0	0	1	0	0
3	1	0	1	0	1	0	1	0
4	1	1	0	1	1	1	0	1

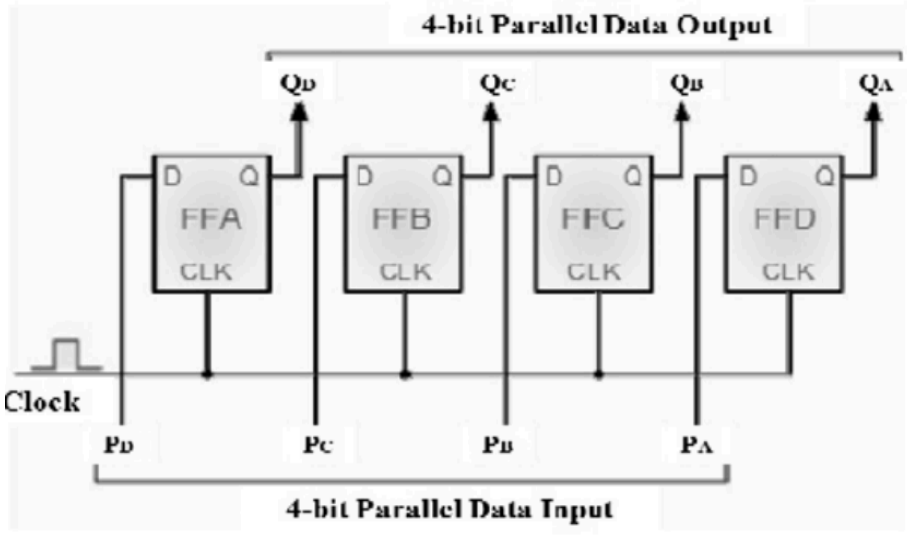
Parallel In Serial Out



Truth table

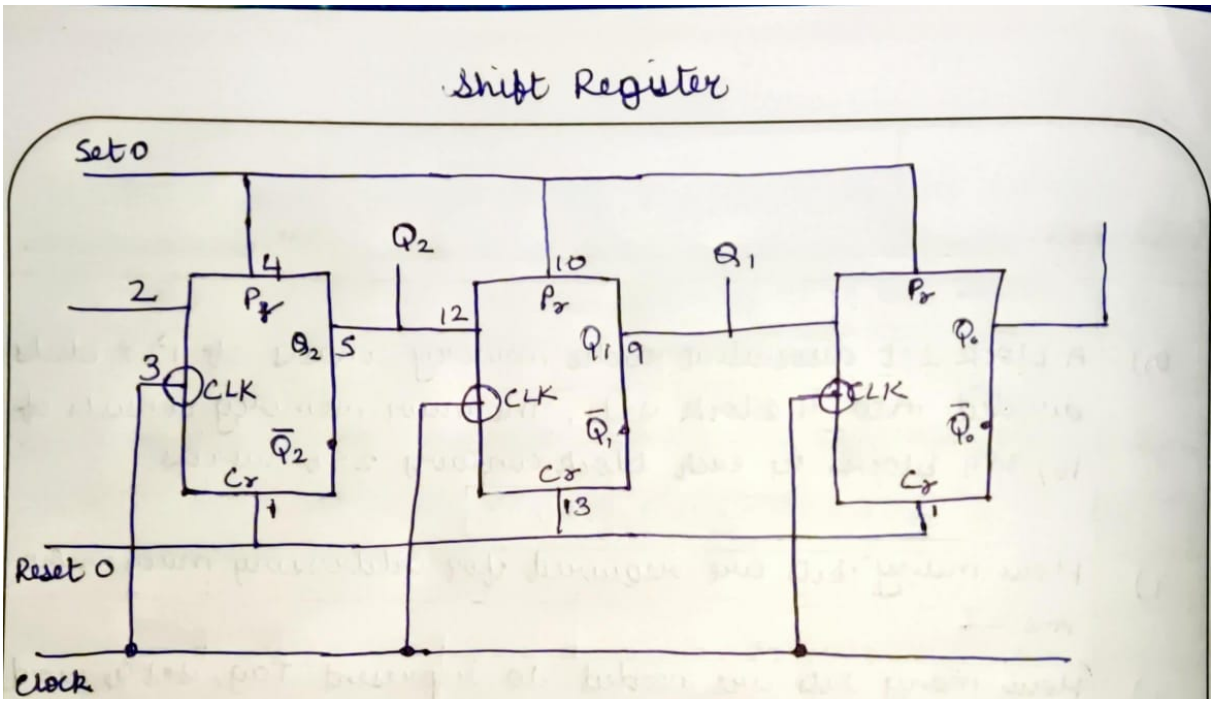
CLK	D3	D2	D1	D0	Q3	Q2	Q1	Q0
0	0	0	0	0	0	0	0	0
1	1	0	0	0	1	0	0	0
2	0	1	0	0	0	1	0	0
3	1	0	1	0	1	0	1	0
4	1	1	0	1	1	1	0	1

Parallel In Parallel Out



Truth table

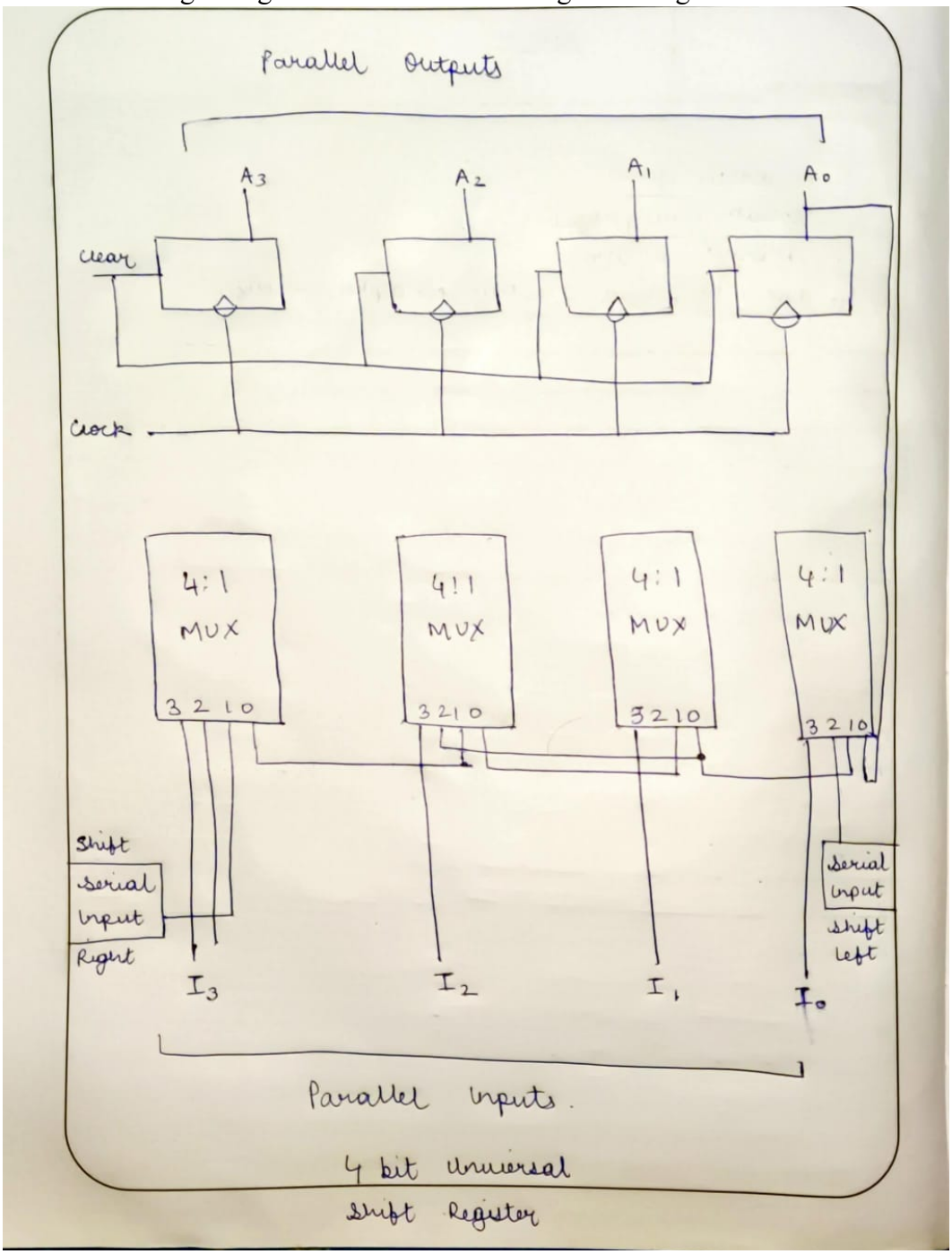
CLK	D3	D2	D1	D0	Q3	Q2	Q1	Q0
0	0	0	0	0	0	0	0	0
1	1	1	0	1	1	1	0	1



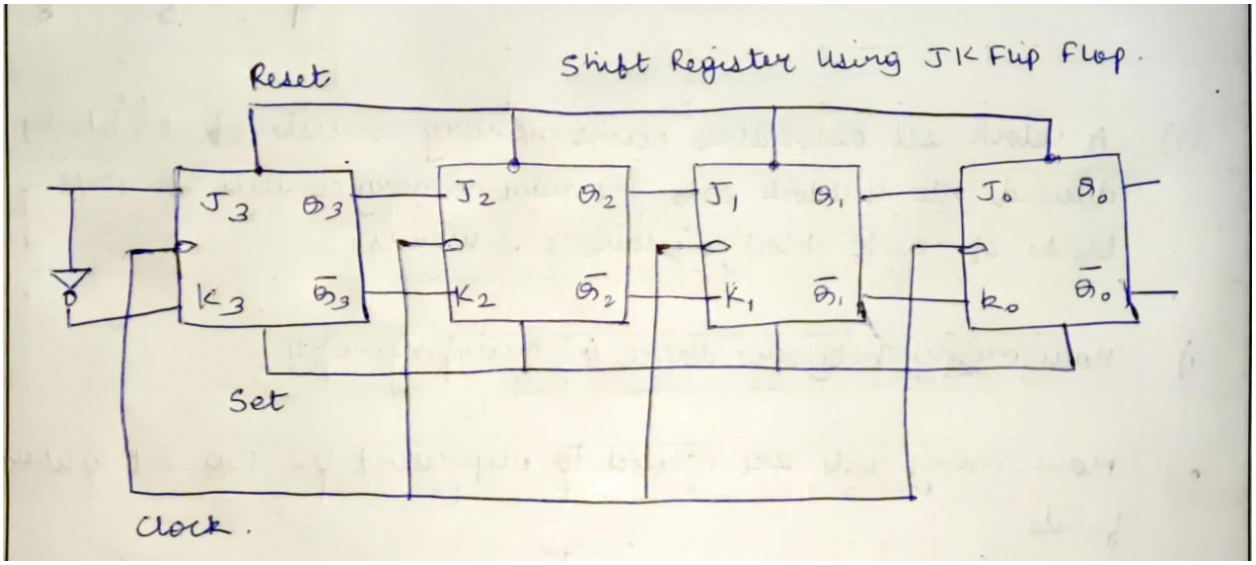
Conclusion: Hence, we studied and successfully implemented.

Post Lab Descriptive Questions

1. Draw logic diagram for universal shift register using 4:1 MUX.



2. Develop the logic diagram for the shift register using JK flip-flop to replace the D flip flop?



3. How many clock pulses are required to enter a byte of data serially into an 8-bit shift register?

The number of individual data latches required to make up a single Shift Register device is usually determined by the number of bits to be stored with the most common being 8-bits (one byte) wide constructed from eight individual data latches. Shift Registers are used for data storage or for the movement of data and are therefore commonly used inside calculators or computers to store data such as two binary numbers before they are added together, or to convert the data from either a serial to parallel or parallel to serial format. The individual data latches that make up a single shift register are all driven by a common clock (CLK) signal making them synchronous devices.