





Experiment / Assignment / Tutorial No. 5

Grade: AA / AB / BB / BC / CC / CD /DD

Signature of the Staff In-charge with date







Batch: A3Roll No.: 16010121045Experiment / assignment / tutorial No.: 5

Title: Flip Flops

Objective:Design of JK Flip flop, D flip flop, T flip flop using NAND Gates & verification of the same flip flop using IC7476

Expected Outcome of Experiment:

CO2: Use different minimization technique and solve combinational circuits, synchronous & asynchronous sequential circuits.

Books/ Journals/ Websites referred:

- VLab Link: <u>http://vlabs.iitkgp.ernet.in/dec/#</u>
- R. P. Jain, "Modern Digital Electronics", Tata McGraw Hill
- M .Morris Mano, "Digital Logic & computer Design", PHI
- A.P.Godse, D.A.Godse, "Digital Logic Design"

Pre Lab/ Prior Concepts:

Flip-flop is the common name given to two-state devices which offer basic memory for sequential logic operations. Flip-flops are heavily used for digital data storage and transfer and are commonly used in banks called "registers" for the storage of binary numerical data.

JK-flip flop: has two inputs, traditionally labeled J and K. IC 7476 is a dual JK master slave flip flop with preset and clear inputs. If J and K are different then the output Q takes the value of J at the next clock edge. If J and K are both low then no change occurs. If J and K are both high at the clock edge, then the output will toggle from one state to the other. It can perform the functions of the set/reset flip-flop and has the advantage that there are no ambiguous states.

D Flip Flop: tracks the input, making transitions with match those of the input D. The D stands for "data"; this flip-flop stores the value that is on the data line. It can be thought of as a basic memory cell. D flip-flop can be made from J-K flip-flop by connecting both inputs through a not gate.

T Flip Flop: T or "toggle" flip-flop changes its output on each clock edge, giving an output which is half the frequency of the signal to the T input. It is useful for constructing binary counters, frequency dividers, and general binary addition devices. It can be made from a J-K flip-flop by tying both of its inputs high.

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Implementation Details:

Procedure

- 1) Locate IC 7476 on Digital trainer kit
- 2) Apply various inputs to J & K pins by means of the output on logic output indicator.
- 3) Connect a pulsar switch to the clock input.
- 4) Connect the J&K as D and T flip flop as shown in diagrams and verify the respective truth tables.



Pin Diagram of IC 7476 JK Master- Slave FF

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Logic Symbol

JKFF



J	K	Q	Q'	Qn+1	Qn+1' n+1
0	0	0	1	0	1
0	0	1	0	1	0
0	1	0	1	0	1
0	1	1	0	0	1
1	0	0	1	1	0
1	0	1	0	1	0
1	1	0	1	1	0
1	1	1	0	0	1

Truth Table

D FF

Truth Table

1	1	1
· L1	Z	

D	O/P
0	0
1	1









Truth Table



Т	O/P
0	1
1	0

Diagram of JK Flip Flop using NAND gates









Lab-Work:











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Conclusion: In this experiment we learnt about various Flip-Flops and their uses. We learnt about their Logic Diagrams and how to implement them.We Learnt the design of JK Flip flop, D flip flop, T flip flop using NAND Gates & verification of the same flip flop using IC7476

Post Lab Descriptive Questions

- 1. How does a JK flip-flop differ from an SR flip-flop in its basic operation?
- The JK flip-flop is a variation or an improvement of the SR flip-flop. The basic difference between SR & JK flip-flop is that JK flip-flop is edge triggered, while SR flip-flop is level triggered.
- The disadvantage of the SR flip-flop is that both inputs shouldn't be HIGH when the clock is triggered. This is considered an invalid input condition, and the resulting output isn't predictable if this condition occurs.
- The main difference between a JK flip-flop and an SR flip-flop is that in the JK flip-flop, both inputs can be HIGH. When both the J and K inputs are HIGH, the Q output is toggled, which means that the output alternates between HIGH and LOW. Thereby the invalid condition which occurs in the SR flip-flop is eliminated.

2. What is use of characteristic and excitation table?

- A characteristic table has the control input (D or T) as the first column, the current state as the middle column, and the next state as the last column. Basically, it tells you how the control bit affects the current state to produce the next state.
- An excitation table has the current state as the first column, the next state as the second column, and the control bit as the third column. Basically, think of this as the state you have (first column), the state you want (second column), and what you must set the control bit (third column) to get the desired state you want. The excitation table is used to implement an FSM

3. How many flip flops due you require storing the data 1101?

4 flip-flops are required for storing a data 1101.

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4. Describe the basic difference between pulse-triggered and edge-triggered flip-flops.

- **Triggering:** This means making a circuit active. Making a circuit active means allowing the circuit to take input and give output. Like for example supposed we have a flip-flop. When the circuit is not triggered, even if you give some input data, it will not change the data stored inside the flip-flop nor will it change the output Q or Q'. The triggering is given in form of a clock pulse or gating signal.
- **Pulse Triggering:** In pulse triggering the circuit will become active when the gating or clock pulse is on a particular level. This level is decided by the designer. We can have a negative level triggering in which the circuit is active when the clock signal is low or a positive level triggering in which the circuit is active when the clock signal is high.
- Edge Triggering: In edge triggering the circuit becomes active at negative or positive edge of the clock signal. For example if the circuit is positive edge triggered, it will take input at exactly the time in which the clock signal goes from low to high. Similarly input is taken at exactly the time in which the clock signal goes from high to low in negative edge triggering. But keep in mind after the input, it can be processed in all the time till the next input is taken.