



**K. J. Somaiya College of Engineering, Mumbai-77**

**Experiment / Assignment / Tutorial No. 4**

**Grade: AA / AB / BB / BC / CC / CD / DD**

**Signature of the Staff In-charge with date**

**K. J. Somaiya College of Engineering, Mumbai-77**

**Batch: A3**

**Roll No.: 16010121045**

**Experiment / assignment / tutorial No.: 4**

**Title: 4 bit Magnitude Comparator**

**Objective:** Design a 2-bit comparator using logic gates and verify 4-bit magnitude comparator using IC 7485

**Expected Outcome of Experiment:**

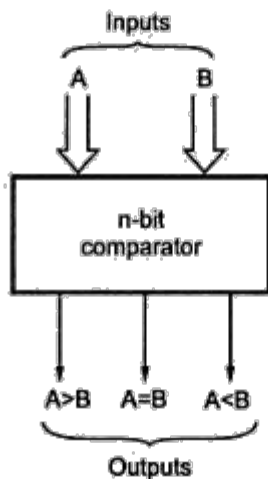
**CO2:** Use different minimization technique and solve combinational circuits, synchronous & asynchronous sequential circuits.

**Books/ Journals/ Websites referred:**

- VLab Link: <http://vlabs.iitb.ac.in/vlabs-dev/labs/dldesignlab/experimentlist.html>
- R. P. Jain, “Modern Digital Electronics”, Tata McGraw Hill
- M .Morris Mano, “Digital Logic & computer Design”, PHI
- [http://elnsite.teilam.gr/ebooks/digital\\_design/lab/dataSheets\\_page/7485.pdf](http://elnsite.teilam.gr/ebooks/digital_design/lab/dataSheets_page/7485.pdf)

**Pre Lab/ Prior Concepts:**

The comparison of two numbers is an operator that determines one number is greater than, less than (or) equal to the other number. A magnitude comparator is a combinational circuit that compares two numbers A and B and determines their relative magnitude. The outcome of the comparator is specified by three binary variables that indicate whether  $A > B$ ,  $A = B$  (or)  $A < B$ .



**Two Bit Magnitude Comparator Implementation Details:**

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### Truth Table

A1	A0	B1	B0	A > B	A = B	A < B
0	0	0	0	0	1	0
0	0	0	1	1	0	0
0	0	1	0	1	0	0
0	0	1	1	1	0	0
0	1	0	0	0	0	1
0	1	0	1	0	1	0
0	1	1	0	1	0	0
0	1	1	1	1	0	0
1	0	0	0	0	0	1
1	0	0	1	0	0	1
1	0	1	0	0	1	0
1	0	1	1	1	0	0
1	1	0	0	0	0	1
1	1	0	1	0	0	1
1	1	1	0	0	0	1
1	1	1	1	0	1	0

**From the Truth Table:**

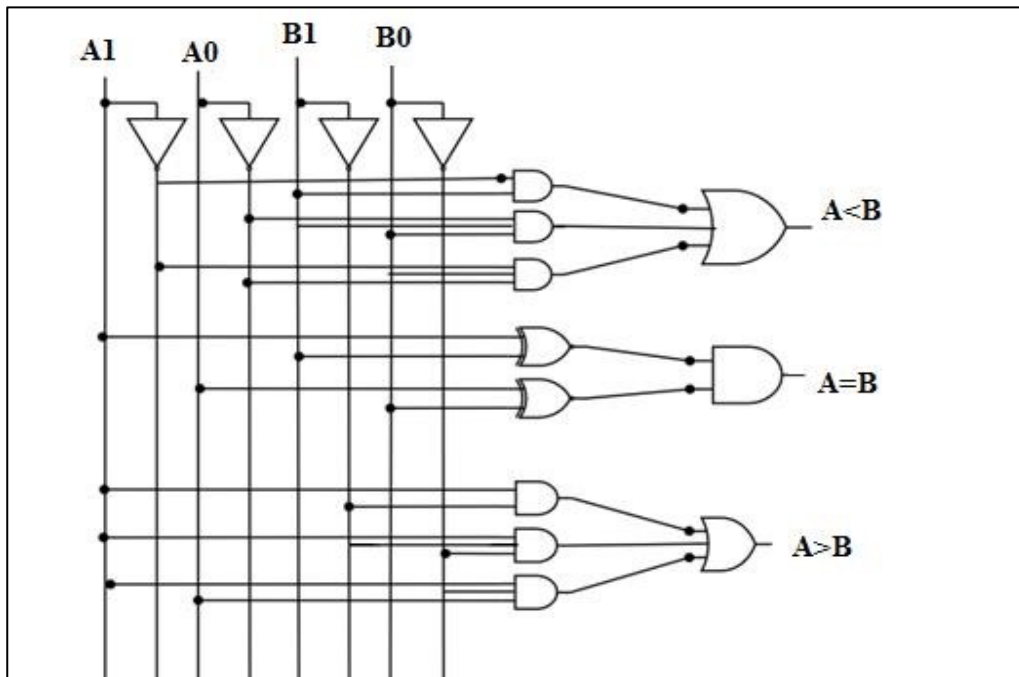
$$(A < B) = A_1' B_1 + A_0' B_1 B_0 + A_1' A_0' B_0$$

$$(A = B) = (A_1 \text{ XOR } B_1) \cdot (A_0 \text{ XOR } B_0)$$

$$(A > B) = A_1 B_1' + A_0 B_1' B_0' + A_1 A_0 B_0'$$

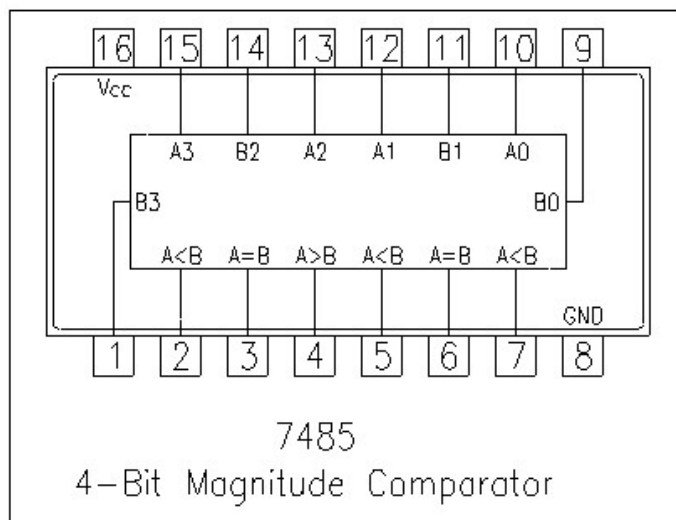
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### Logic Diagram of 2 bit Comparator



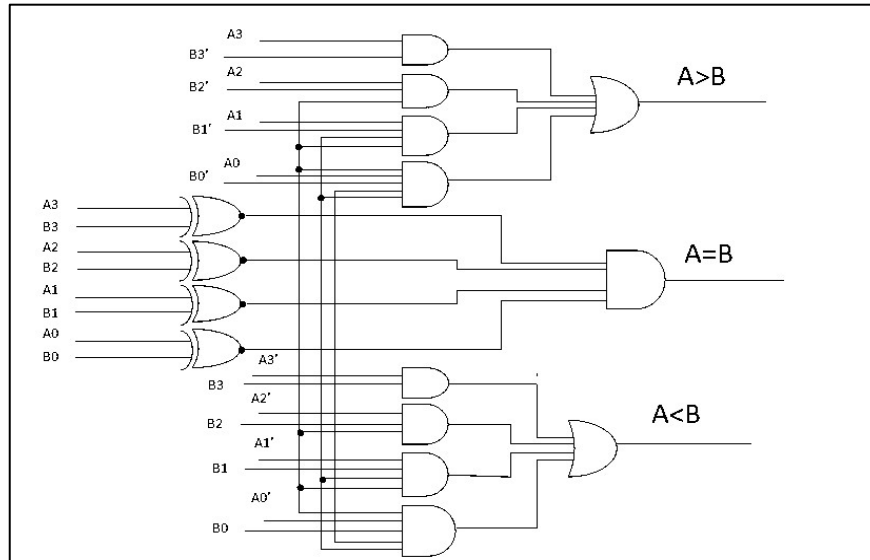
### Four Bit Magnitude Comparator Implementation Details

#### Pin Diagram of IC 7485



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### Logic Diagram of IC 7485



### Comparing Table

INPUTS of 4 bit Comparator				OUTPUT		
A3, B3	A2, B2	A3, B3	A2, B2	A3, B3	A2, B2	A3, B3
A3 > B3	X	X	X	H	L	L
A3 < B3	X	X	X	L	H	L
A3 = B3	A2 > B2	X	X	H	L	L
A3 = B3	A2 < B2	X	X	L	H	L
A3 = B3	A2 = B2	A1 > B1	X	H	L	L
A3 = B3	A2 = B2	A1 < B1	X	L	H	L
A3 = B3	A2 = B2	A1 = B1	A0 > B0	H	L	L
A3 = B3	A2 = B2	A1 = B1	A0 < B0	L	H	L
A3 = B3	A2 = B2	A1 = B1	A0 = B0	H	L	L
A3 = B3	A2 = B2	A1 = B1	A0 = B0	L	H	L
A3 = B3	A2 = B2	A1 = B1	A0 = B0	L	L	H

Where H = High Output, L = Low Output, X = Don't Care

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Lab-Work:

Exp 4 a : Comparator  
4 bit

Pangat Singh  
16010121045

Comp O/P	Cascady I/P			O/P
	$I_{A>B}$	$I_{A=B}$	$I_{A<B}$	$O_{A>B}$ $O_{A=B}$ $O_{A<B}$
$A > B$	X	X	X	1 0 0
$A = B$	1	0	0	1 0 0
	0	0	1	0 0 1
	X	1	X	0 1 0
	1	0	1	0 0 0
	0	0	0	1 0 1
$A < B$	X	X	X	0 0 1

↓  
Don't care.

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**Conclusion:** Through this experiment we learnt the concept of comparators – 1 bit, 2 bit and 4 bits. We also learnt to implement them through logic diagrams and truth tables.

### Post Lab Descriptive Questions

1. Design a 1- bit magnitude comparator using logic gates.

A	B	f(A>B)	f(A=B)	f(A<B)
0	0	0	1	0
1	0	1	0	0
0	1	0	0	1
1	1	0	1	0

**From the truth table:**

Equation of  $A > B = A.B'$

Equation of  $A < B = A'.B$

Equation of  $(A = B) = A'.B' + A.B = A \text{ XNOR } B = (A.B' + A'.B)'$

