**Experiment / Assignment / Tutorial No. 2**

**Grade: AA / AB / BB / BC / CC / CD /DD**

**Signature of the Staff In-charge with date**

| Batch: A3 | Roll No.: 16010121045 | Experiment / assignment / tutorial No.: 2 |
|---|---|---|

**Title:** Binary Adders and Subtractors

---

**Objective:** To implement half and full adder–subtractor using gates and IC 7483

---

**Expected Outcome of Experiment:**

**CO2:** Use different minimization technique and solve combinational circuits, synchronous & asynchronous sequential circuits.

---

**Books/ Journals/ Websites referred:**

- **VLab Link:** http://vlabs.iitb.ac.in/vlabs-dev/labs/dldesignlab/experimentlist.html
- R. P. Jain, "Modern Digital Electronics", Tata McGraw Hill
- M .Morris Mano, "Digital Logic & computer Design", PHI
- http://physics.niser.ac.in/labmanuals/sem5/elect/7_ADDER%20SUBTRACTOR%20CIRCUITS.pdf

**Pre Lab/ Prior Concepts:**

**Adder:** Addition of two binary digits is most basic operation performed by the digital computer. There are two types of adder:

- Half adder
- Full adder

**Half Adder:** Half adder is combinational logic circuit with two inputs and two outputs. It is the basic building block for addition of two single bit numbers.

**Full adder:** A half adder has a provision not to add a carry coming from the lower order bits when multi bit addition is performed. for this purpose a third input terminal is added and this circuits is to add A,B,C where A and B are the nth order bits of the number A and B respectively and C is the carry generated from the addition of (n-1) order bits. This circuit is referred to as full adder.

**Subtractor:** Subtraction of two binary digits is one of the most basic operations performed by digital computer .there are two types of subtractor:

- Half subtractor
- Full subtractor

**Half subtractor:** Logic circuit for the subtraction of B from A where A,B are 1 bit numbers is referred to as half subtract or .the subtract or process has two input and difference and borrow are the two outputs.

**Full subtractor:** As in the case of the addition using logic gates, a full subtractor is made by combining two half-sub tractors and an additional OR-gate. A full subtractor has the borrow in capability (denoted as $BOR_{IN}$) and so allows cascading which results in the possibility of multi-bit subtraction.

**IC 7483**

For subtraction of one binary number from another, we do so by adding 2's complement of the former to the latter number using a full adder circuit.

IC 7483 is a 16 pin, 4-bit full adder. This IC has a provision to add the carry output to transfer and end around carry output using Co and C4 respectively.

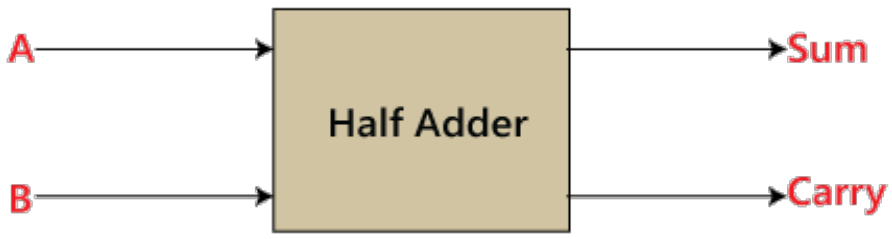
**2's complement:** 2's complement of any binary no. can be obtained by adding 1 in 1'scomplement of that no.

e.g. 2's complement of $+(10)_{10}$ =1010is

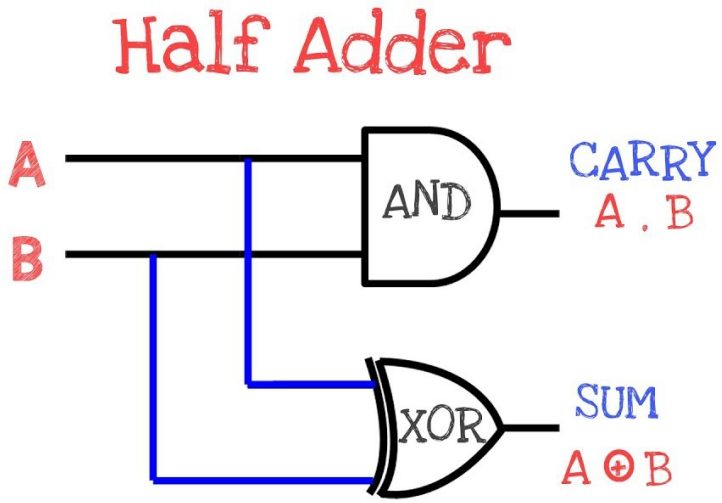
| | |
|---|---|
| 1C of 1010 | 0101 |
| | + 1 |
| $-(10)_{10}$ | 0110 |

In 2's complement subtraction using IC 7483, we are representing negative number in 2's complement form and then adding it with 1st number.

**Implementation Details:**
**Half Adder Block Diagram**



**Half Adder Circuit**



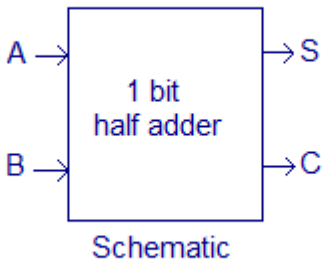

**Truth Table for Half Adder**

| Inputs | | Outputs | |
|---|---|---|---|
| **A** | **B** | **A** | **B** |
| 0 | 0 | 0 | 0 |
| 0 | 1 | 0 | 1 |
| 1 | 0 | 1 | 0 |
| 1 | 1 | 1 | 1 |

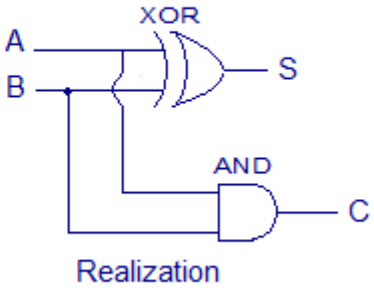
**From the truth table (with steps):**

| Inputs | | Outputs | |
|---|---|---|---|
| A | B | S | C |
| 0 | 0 | 0 | 0 |
| 1 | 0 | 1 | 0 |
| 0 | 1 | 1 | 0 |
| 1 | 1 | 0 | 1 |

Truth table

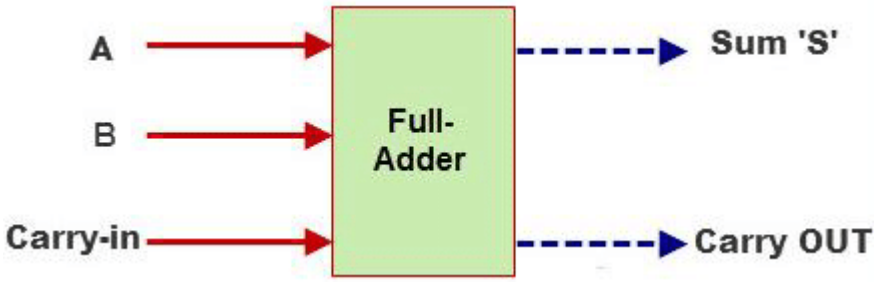



Schematic

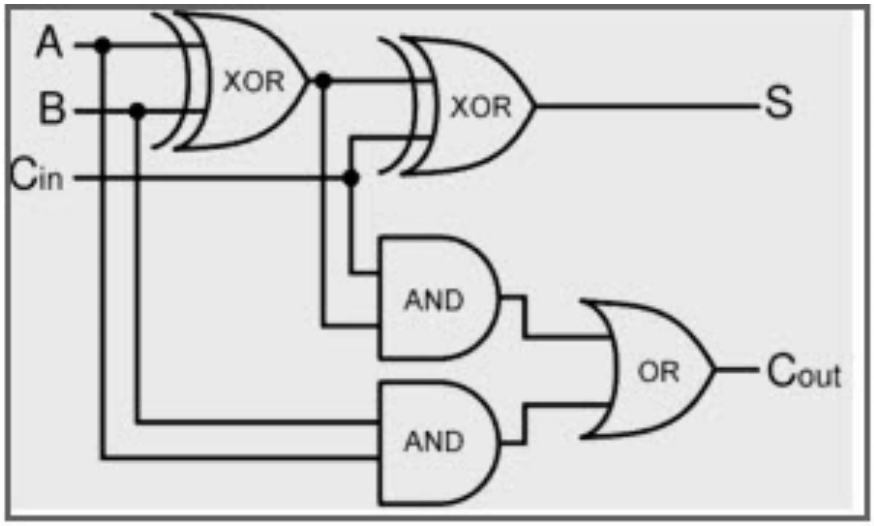



Realization

**Full Adder Block Diagram**




**Full Adder Circuit**



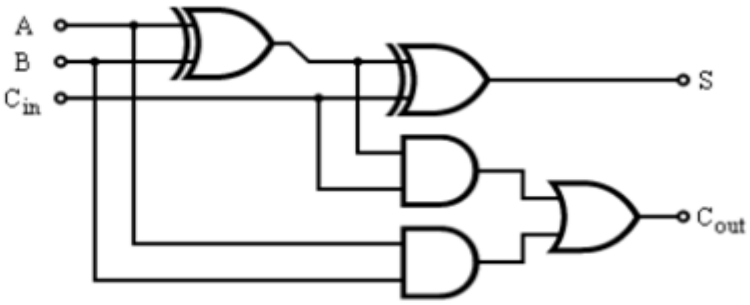

**Truth Table for Full Adder**

| Inputs | | | Outputs | |
|---|---|---|---|---|
| A | B | $C_{in}$ | Sum | Carry |
| 0 | 0 | 0 | 0 | 0 |
| 0 | 0 | 1 | 1 | 0 |
| 0 | 1 | 0 | 1 | 0 |
| 0 | 1 | 1 | 0 | 1 |
| 1 | 0 | 0 | 1 | 0 |
| 1 | 0 | 1 | 0 | 1 |
| 1 | 1 | 0 | 0 | 1 |
| 1 | 1 | 1 | 1 | 1 |

**From the truth table (with steps):**

| Full Adder Truth Table | | | | |
|---|---|---|---|---|
| A | B | Cin | Cout | Sum |
| 0 | 0 | 0 | 0 | 0 |
| 1 | 0 | 0 | 0 | 1 |
| 0 | 1 | 0 | 0 | 1 |
| 1 | 1 | 0 | 1 | 0 |
| 0 | 0 | 1 | 0 | 1 |
| 1 | 0 | 1 | 1 | 0 |
| 0 | 1 | 1 | 1 | 0 |
| 1 | 1 | 1 | 1 | 1 |

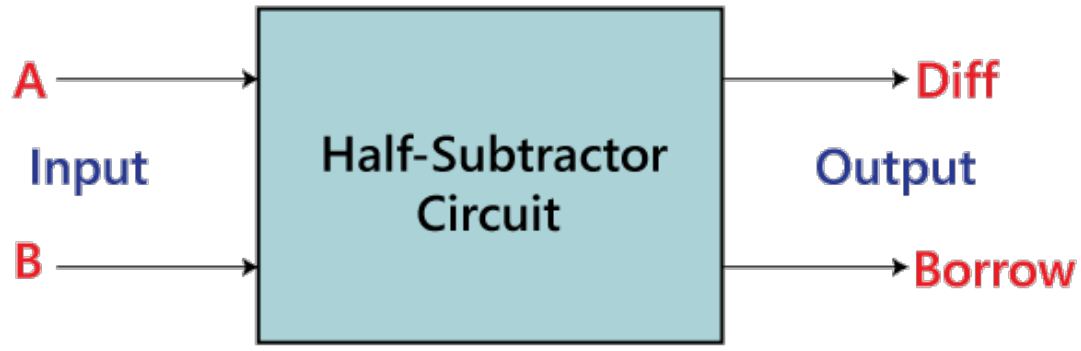
**VHDL Code Full adder Circuit**



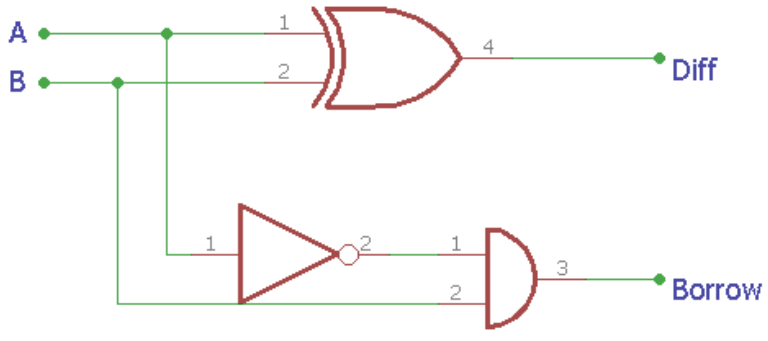

Full-Adder

www.androiderode.com

**Half Subtractor Block Diagram**




**Half Subtractor Circuit**



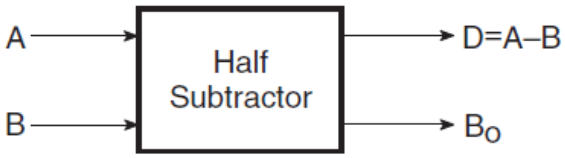

Half-Subtractor Circuit

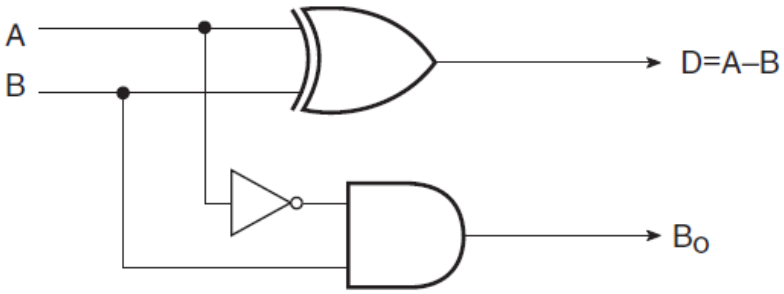
**Truth Table for Half Subtractor**

| A | B | DIFFERENCE (D) | BORROW(Bo) |
|---|---|---|---|
| 0 | 0 | 0 | 0 |
| 0 | 1 | 1 | 1 |
| 1 | 0 | 1 | 0 |
| 1 | 1 | 0 | 0 |

**From the truth table (with steps) :**

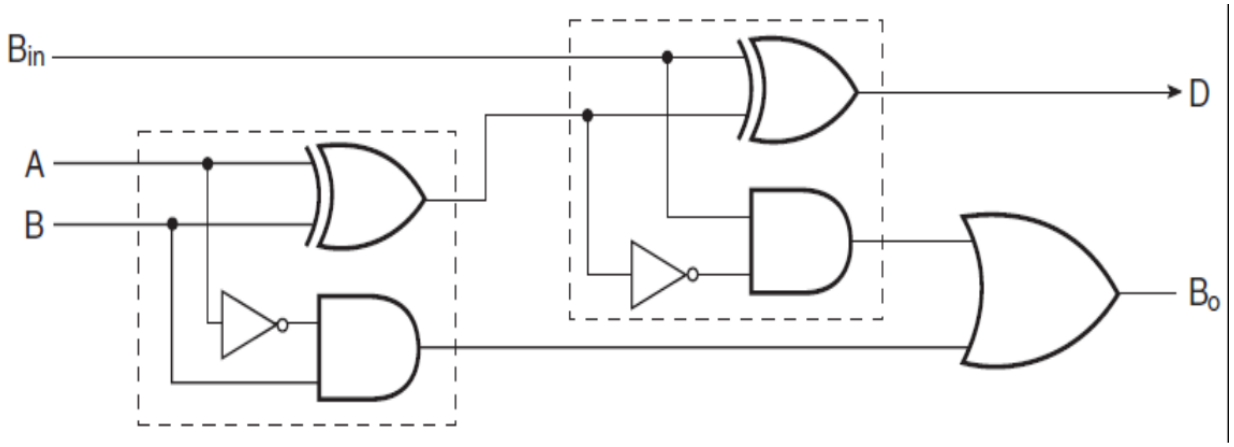
| A | B | D | $B_o$ |
|---|---|---|---|
| 0 | 0 | 0 | 0 |
| 0 | 1 | 1 | 1 |
| 1 | 0 | 1 | 0 |
| 1 | 1 | 0 | 0 |




**Full Subtractor Block Diagram**

**Full Subtractor Circuit**




**Truth Table for Full subtractor**

| A | B | BIN | D | BOROUT |
|---|---|---|---|---|
| 0 | 0 | 0 | 0 | 0 |
| 0 | 0 | 1 | 1 | 1 |
| 0 | 1 | 0 | 1 | 1 |
| 0 | 1 | 1 | 0 | 1 |
| 1 | 0 | 0 | 1 | 0 |
| 1 | 0 | 1 | 0 | 0 |
| 1 | 1 | 0 | 0 | 0 |
| 1 | 1 | 1 | 1 | 1 |

**From the truth table (with steps):**

Differenc = A'B'Bin + A'BBin' + AB'Bin' + ABBin
Borrow out= A'B + A'Bin + BBin

| Input | | | | | | | | | | Output | |
|---|---|---|---|---|---|---|---|---|---|---|---|
| A | B | Bin | A ⊕ B = C | ~A = E | E.B = F | Bin⊕ C = G | ~C = F | F.Bin = H | F + H = I | D | $Borr_{out}$ |
| 0 | 0 | 0 | 0 | 1 | 0 | 0 | 1 | 0 | 1 | 0 | 0 |
| 0 | 0 | 1 | 0 | 1 | 0 | 1 | 1 | 1 | 1 | 1 | 1 |
| 0 | 1 | 0 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 1 | 1 |
| 0 | 1 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 1 |
| 1 | 0 | 0 | 1 | 0 | 0 | 1 | 0 | 0 | 0 | 1 | 0 |
| 1 | 0 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 1 | 1 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 1 | 0 | 0 |
| 1 | 1 | 1 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 1 | 1 |

**IC 7483**
**Procedure:**

1) Locate the IC 7483 and 4-not gates block on trainer kit.
2) Connect 1st input no. to A4-A1 input slot and 2nd (negative) no. to B4-B1 through 4-not gates (1C of 2nd no.)
3) Connect high input to Co so that it will get added with 1C of 2nd no. to get 2C.
4) Connect 4-bit output to the output indicators.
5) Switch ON the power supply and monitor the output for various input combinations.

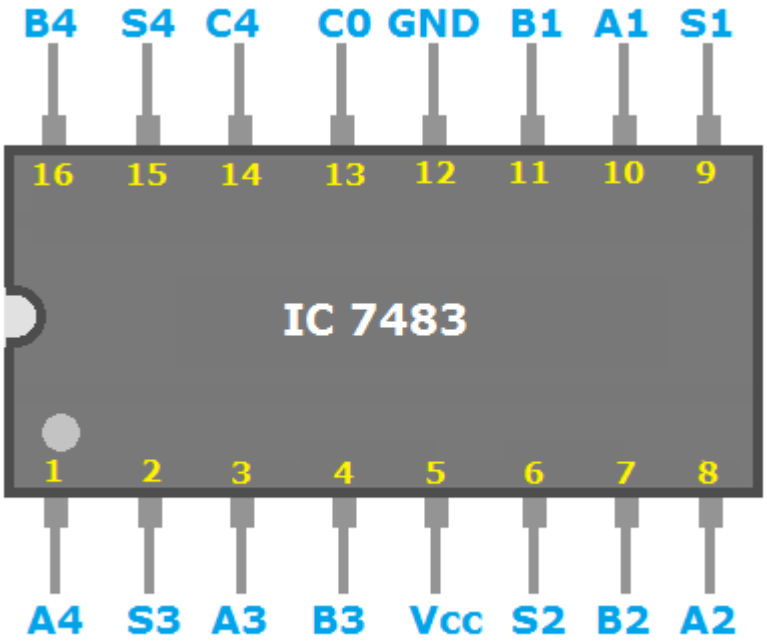
**Example:**

1) $7_{10} - 2_{10} = 5_{10}$

| | |
|---|---|
| 7 | 0111 |
| 2 | 0010 |
| 1'C of 2 | 1101 |
| | + 1 |
| 2'C of 2 | 1110 |

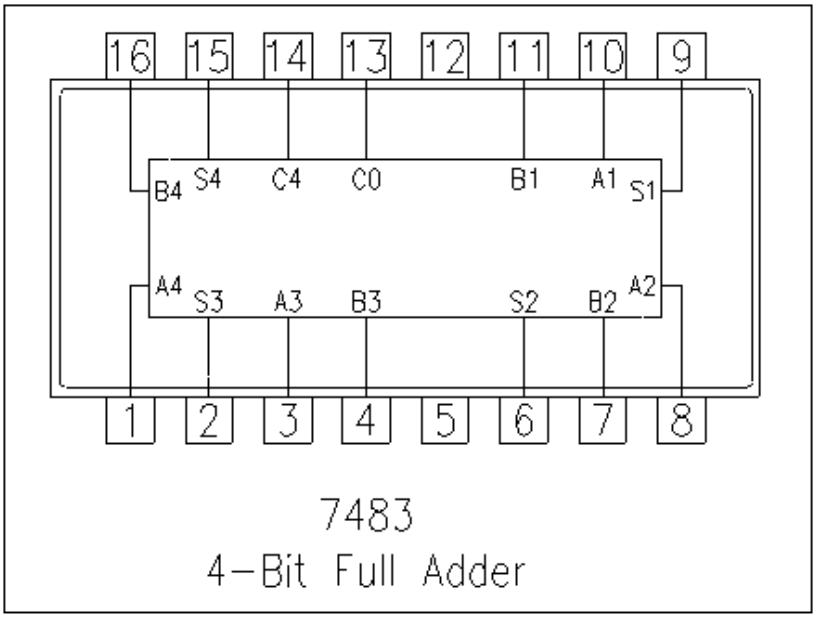
0111 + 1110
1 0101

**Pin Diagram IC7483**

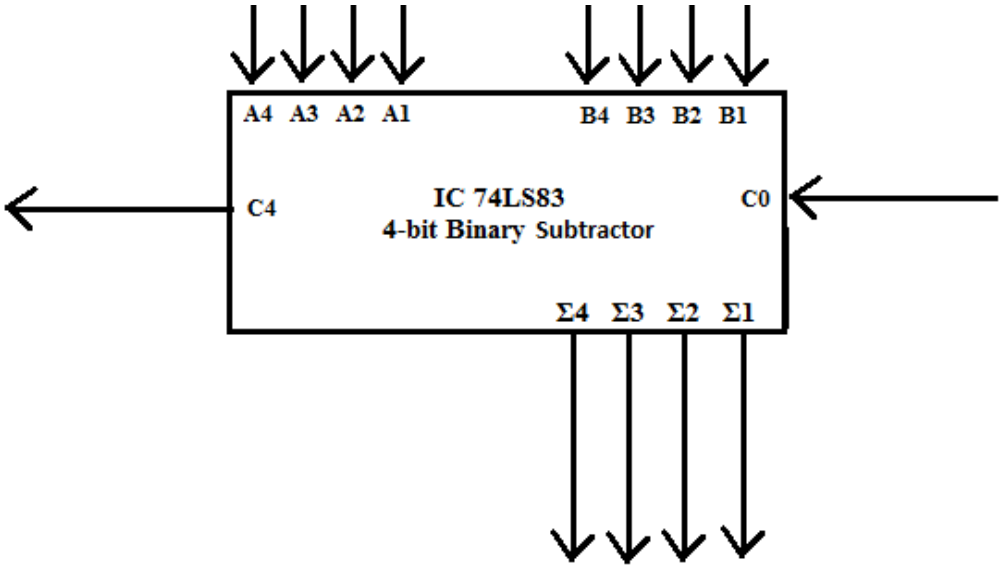



IC 7483 Pin Diagram

**Adder**



**Subtractor**




**Conclusion:** Thus the circuits of binary adder and sub tractors were studied on the IC kit using Connectors and tested using sample values.

**Post Lab Descriptive Questions**

1. What is difference between half and full adder, half and full subtractor?

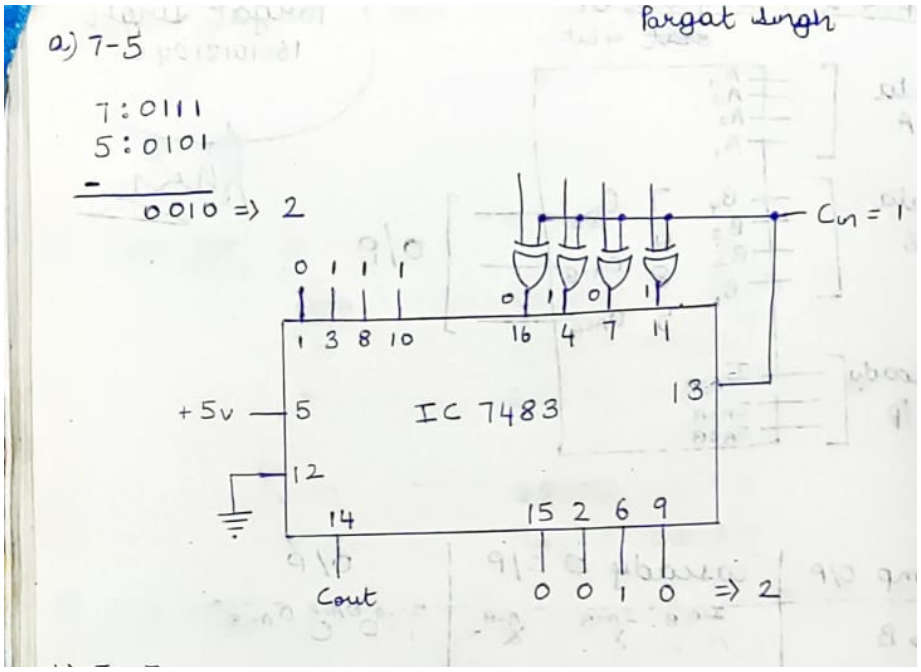
A) Difference between half and full adder

| Half Adder | Full Adder |
|---|---|
| Half adder accepts two binary digits on it's inputs and produce two binary digits outputs, a sum bit and a carry bit | The full adder accepts two input bits and an input carry and generates a sum output and an output carry |
| Half adder is easier to implement. | It is more difficult as it needs two half adders to implement |
| Half adder can add only two input bits (A and B) and has nothing to do with carry if there is only one input, that means the binary addition process is not complete, thus it is called half adder. | Full adder can add a 3 bit number (A,B,Cin) A and B are the operands and Cin is the carry from the previous less significant stage. |

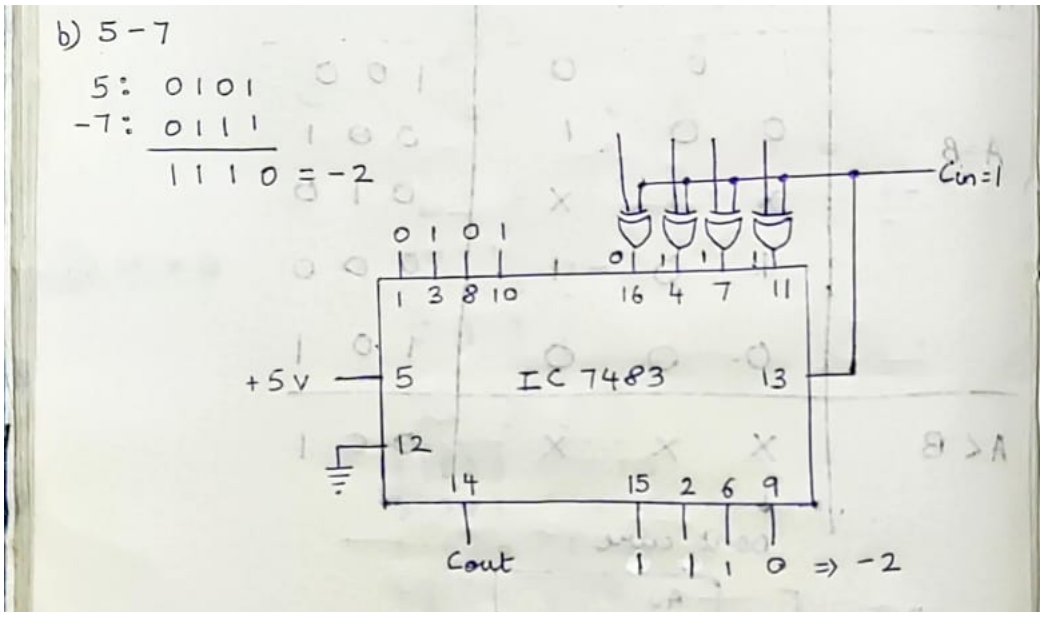
B) Difference between half and full subtractor

<table>
<tr><th>Half Subtractor</th><th>Full Subtractor</th></tr>
<tr><td>1. It is a combinational circuit which is used to perform subtraction of two bits</td><td>. It is a combinational circuit which is used to perform subtraction of three bits</td></tr>
<tr><td>2. It has two inputs (A,B) and two output D(Difference) and B(Borrow).</td><td>It has input A(number) B(subtractor) and Bin (Borrow) from previous stage. And the outputs are D (Difference) and B (Borrow)</td></tr>
<tr><td>3.<br><br>Truth table :<br><br><table><tr><td>A</td><td>B</td><td>D</td><td>B</td></tr><tr><td>0</td><td>0</td><td>0</td><td>0</td></tr><tr><td>0</td><td>1</td><td>1</td><td>1</td></tr><tr><td>1</td><td>0</td><td>1</td><td>0</td></tr><tr><td>1</td><td>1</td><td>0</td><td>0</td></tr></table></td><td>3.<br><br>Truth table:<br><br><table><tr><td>A</td><td>B</td><td>Bin</td><td>D</td><td>Bout</td></tr><tr><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td></tr><tr><td>0</td><td>0</td><td>1</td><td>1</td><td>1</td></tr><tr><td>0</td><td>1</td><td>0</td><td>1</td><td>1</td></tr><tr><td>0</td><td>1</td><td>1</td><td>0</td><td>1</td></tr><tr><td>1</td><td>0</td><td>0</td><td>1</td><td>0</td></tr><tr><td>1</td><td>0</td><td>1</td><td>0</td><td>0</td></tr><tr><td>1</td><td>1</td><td>0</td><td>0</td><td>0</td></tr><tr><td>1</td><td>1</td><td>1</td><td>1</td><td>1</td></tr></table></td></tr>
</table>

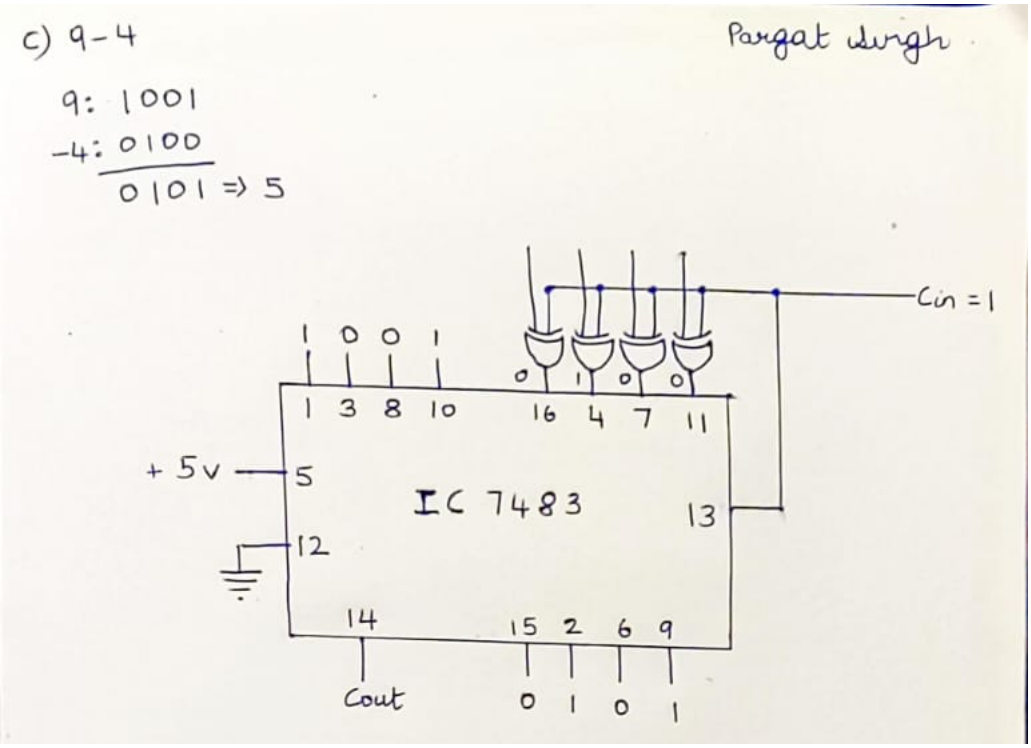
2. **Perform the following Binary subtraction with the help of appropriate ICs:**
   a) **7-5**



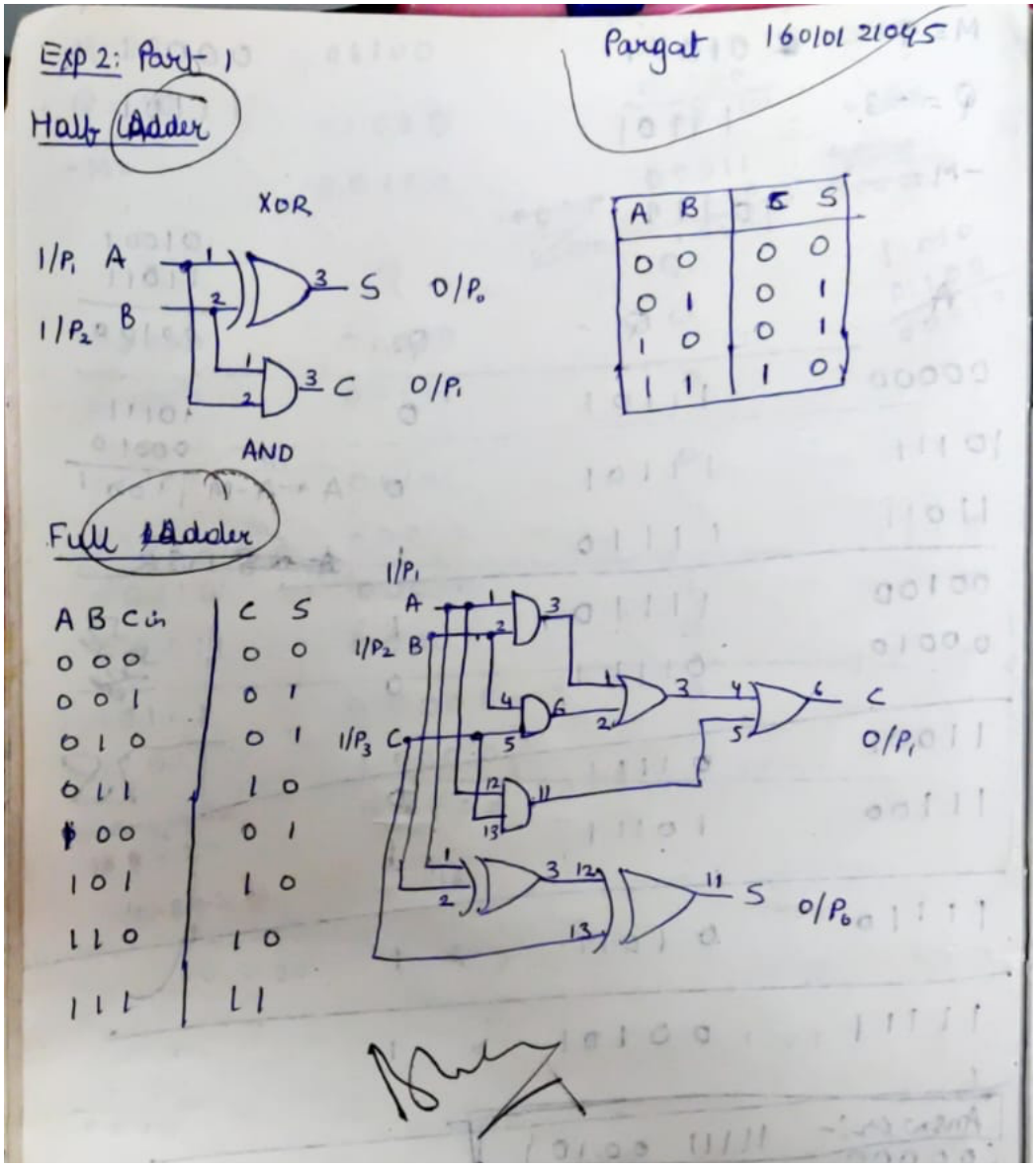

   b) **5-7**



**c) 9-4**


c) 9-4
Pargat Singh
9: 1001
-4: 0100
0101 => 5
1 0 0 1
1 3 8 10
0 1 0 0
16 4 7 11
Cin = 1
+5v
5
IC 7483
13
12
14
15 2 6 9
Cout
0 1 0 1

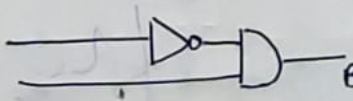
**Lab Work:**


EXP 2: Part-1
Pargat 160101 21045
Half Adder
XOR
I/P1 A
I/P2 B
S
O/P0
C
O/P1
AND
A B S C
Full Adder
A B Cin
C S
I/P1
I/P2 B
I/P3 C
O/P1
O/P0

## Half subtractor

$A_0$
$- B_0$

| $A_0$ | $B_0$ | $D_0$ | $BR_0$ |
|---|---|---|---|
| 0 | 0 | 0 | 0 |
| 0 | 1 | 1 | 0 |
| 1 | 0 | 1 | 1 |
| 1 | 1 | 0 | 0 |




XOR

$\bar{A} \cdot B$

## Full subtractor

$A_i$
$- B_i \quad BR_{in}$
$BR_{out} \quad D_{out}$

| $A_i$ | $B_i$ | $BR_{in}$ | $D_{out}$ | $BR_{out}$ |
|---|---|---|---|---|
| 0 | 0 | 0 | 0 | 0 |
| 0 | 0 | 1 | 1 | 1 |
| 0 | 1 | 0 | 1 | 1 |
| 0 | 1 | 1 | 0 | 1 |
| 1 | 0 | 0 | 1 | 0 |
| 1 | 0 | 1 | 0 | 0 |
| 1 | 1 | 0 | 0 | 0 |
| 1 | 1 | 1 | 1 | 1 |